BMPS Application Guideline

File Name BMPS05001 Draft 4

THE GLOBAL ELECTRONIC PACKAGING NETWORK

NORTHEN AMERICA EUROPE ASIA

HDP USER GROUP INTERNATIONAL, INC.

i Document History

Public Version Date

ii Acknowledgements

The following people associated with HDP User Group have prepared this BMPS Application Guideline:

- Per Lindman, Ericsson Power Modules
- Lars Thorsell, PowerBrand - Consulting
- Ruben Bergman, HDP User Group
-

The following organizations have endorsed this BMPS Application Guideline:

- PSMA?
- EPSMA?
- DOSA?
- POLA?

iii Supporters

This section will be updated after reviews

iiii Disclaimer

Warranties

THIS INFORMATION IS PROVIDED "AS IS" WITHOUT WARRANTY OF ANY KIND, EITHER EXPRESSED OR IMPLIED, INCLUDING, BUT NOT LIMITED TO, THE IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, OR NON-INFRINGEMENT.

REFERENCES TO CORPORATIONS, THEIR SERVICES AND PRODUCTS, ARE PROVIDED "AS IS" WITHOUT WARRANTY OF ANY KIND, EITHER EXPRESSED OR IMPLIED. IN NO EVENT SHALL HDP USER GROUP INTERNATIONAL, INC. BE LIABLE FOR ANY SPECIAL, INCIDENTAL, INDIRECT OR CONSEQUENTIAL DAMAGES OF ANY KIND, OR ANY DAMAGES WHATSOEVER RESULTING FROM LOSS OF USE, DATA OR PROFITS, WHETHER OR NOT ADVISED OF THE POSSIBILITY OF DAMAGE, AND ON ANY THEORY OF LIABILITY, ARISING OUT OF OR IN CONNECTION WITH THE USE OR PERFORMANCE OF THIS INFORMATION.

Descriptions of, or references to, products, services or publications within this document does not imply endorsement of that product, service or publication. HDP User Group International, Inc. makes no warranty of any kind with respect to the subject matter included herein, the products listed herein, or the completeness or accuracy of the information. HDP User Group International, Inc. specifically disclaims all warranties, express, implied or otherwise, including without limitation, all warranties of merchantability and fitness for a particular purpose.

THIS PUBLICATION COULD INCLUDE TECHNICAL INACCURACIES OR TYPOGRAPHICAL ERRORS. CHANGES MAY BE PERIODICALLY MADE TO THE INFORMATION HEREIN.

Table of contents

i Document History
ii Acknowledgements
iii Supporters
iiii Disclaimer

Contents

1 Introduction

Time to market is shorter, with ever increasing pressure on the power system designer to deliver cost effective power systems that are reliable, easy to manufacture, and pass regulatory qualification on the first attempt. It's rarely acceptable to wait several months or even years for the development of customized power system solutions. System integrators and equipment manufacturers demand denser, more reliable power systems that are truly designed for manufacturing, but with a reduced development schedule and budget. The above can be a difficult challenge. This overview of modern power system design and the technologies and components available to support it, is an endeavor to assist the designer with the above challenge.

Since mid 80th the development of miniaturized switching power supplies has brought on the practical implementation of decentralized power systems utilizing standardized Board Mounted Power Supplies (BMPS) i.e. Distributed Power Architectures (DPA). BMPS in this context means on-board DC/DC regulators and DC/DC converters, sometimes referred to as DC/DC power modules or simply power modules or converters.

However, the selection of such standardized BMPS is not always easy due to the wide range of products now available and the sometime confusing performance claims made. Some suppliers emphasize power density, others switching frequency or converter topology, still others efficiency.

Which is most important? How does the reliability of decentralized power architectures compare with centralized systems? What factors determine reliability? How are small BMPS packaged within a system? What provisions are required for cooling? Why can't the maximum rated power of some converters be realized in practical systems? What are the real costs associated with power converter failures? Even though the newly available technologies and products offer exciting benefits, the list of questions such as those above seems to keep growing. The purpose here is to answer these questions and others, and provide a practical source of information for the power system designer - information that is based upon experience with actual systems and applications rather than just textbook formulas. It is our hope that the information contained here will be helpful in selecting a power system architecture that meets the needs of the product, selecting the appropriate BMPS or components with which to implement the system, and in applying the selected BMPS and components correctly. The result should be a design that meets the product needs, requires minimal design and qualification time, and has an acceptable manufacturing cost.

This Guideline is aimed at facilitating the communication between suppliers of BMPS and their customers, which are system integrators and EMS providers. The guideline provides easy access to the key items of information for:

- System integrators when they are designing printed wiring board assemblies with BMPS
- EMS providers when they are assembling printed wiring boards with BMPS
- Power supply manufacturers when they are designing and manufacturing BMPS

The guideline will first give an overview of power system requirements, starting at the circuit level and extending into system controls and packaging and regulatory requirements. Next, power system architectures in a generalized way are addressed before focusing in on decentralized (or distributed) power architectures. Tradeoffs between custom and standard power converters from a design and system management point of view will be discussed followed by an overview of commonly used converter topologies and their characteristics. It then look in more detail at the design and implementation of decentralized power systems including electrical design, thermal design, and other product considerations. Reliability is ever more important in today's power systems, and a section is devoted to several aspects of power system reliability, including prediction, design practices, and how reliability is affected by power architecture and hardware choices. The 'bottom line' for most system manufacturers is cost. A separate chapter is devoted to cost analysis techniques useful for decentralized power system design, considering a product's 'life cycle cost', which consists not only of price, manufacturing and installment costs, but also very important indirect costs such as spare parts, service action and time-to-market. Furthermore, it's shown how reliability information can be accounted for when doing cost

analysis. There is also a section that attempts to clear the clouds and uncertainties regarding the design for conducted emissions compatibility, which is one of the more important design challenges. A section describing selection criteria for BMPS follows this. Finally a list of recent practical references is included for those readers wishing to expand upon the content supplied here.
The guidelines are primarily based upon Ericsson Power Modules The **POWER**BOOK , 4th revised edition with it's first edition issued 1993.

The final content has been gathered and reviewed by the BMPS Reference Group formed out of members from EPSMA, PSMA and HDP User Group. Acknowledgements to other contributing companies are separately listed under *jj Acknowledgements*

(>1.5 m/s). The diagnostic strategy for the DC part of the system becomes very simple – there isn't any! There are no separate power converters to diagnose or replace. When a circuit board fails, the associated power conversion function automatically gets replaced.

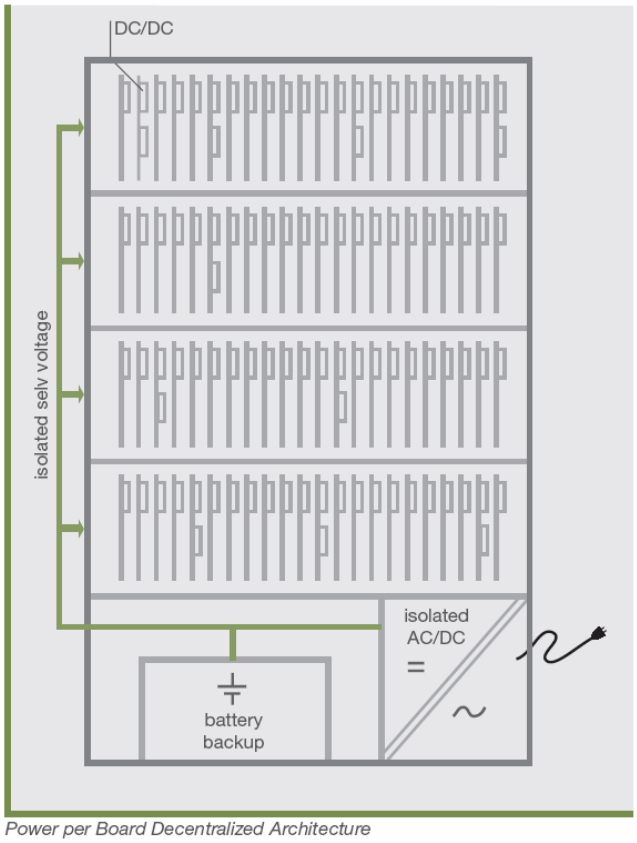


Figure 2.2.5.4

In a system such as this, the DC/DC power converters or BMPS essentially become components on the circuit boards, a goal that has been eluding power system designers until recently. For this approach to be economically viable, the modules must be very reliable, very small, and inexpensive.

2.3 Decentralized Power Architectures

The advent of standard modular power converter solutions has provided a substantial benefit to the power system designer. No longer must there be concerns about such things as converter circuit topology selection, circuit design, manufacturing sourcing, component selection, and a host of other issues related to design and production of a custom switching regulator. Instead, the designer can choose with confidence from a selection of standard BMPS that are already proven designs with agency approvals and qualifications in place.

2.3.1 Characteristics of Decentralized Power Architectures

In a previous chapter, we defined the various types of power architectures, and gave several examples of how such architectures can be implemented in products. We saw that decentralized approaches resolve many of the problems of the more centralized designs. But the decentralized approach will only be economically viable if commercially available DC/DC power modules have the proper characteristics. In this section, we will discuss the required technologies that make this possible. We will also explore in more detail some of the advantages of decentralized architectures. In this discussion, we will assume the 'Power per Board' implementation, which is the ultimate execution of the concept of decentralized power implemented with distributed BMPS. Most of the advantages described will also apply, sometimes to a lesser degree, to 'Power per Function' and 'Power per Shelf" decentralized architectures.

2.3.2 Viability of Decentralized Power Architectures

Decentralized power is not a new concept. Many engineers and system designers recognized its inherent simplicity and advantages long ago. Unfortunately, it was not extensively used until recently due to the lack of suitable technology. In order to share circuit board real estate with load circuitry and do so economically, the power converter must possess the following technology-driven attributes: small footprint, low profile, high efficiency, and superior electrical performance, manufacturing compatibility, high reliability low cost and low weight.

All of these attributes are now available and are exemplified in several manufacturers BMPS product lines. From the industry standard SMT packaging of molded products to the high power open frame so called Bricks with extremely high efficiency and power density, there are products that address all of these requirements. This broad product selection allows the construction of high performance decentralized power systems that meet high performance requirements and aggressive cost targets.

2.3.3 Advantages of Decentralized Power Architectures

2.3.3.1 Better Electrical Performance

Placing the final stage of power conversion close to the load circuitry provides some stunning performance advantages. The DC distribution system becomes much shorter and simpler, eliminating power losses in the distribution network. Better dynamic response performance is also achieved due to the lower inductance between the converter and its load. The proximity to the load also allows for good voltage regulation without the need for remote sensing in many applications. The VRM implementation for powering the processor chip in a personal computer, as described in the previous chapter, is a good example of how decentralized approaches can achieve levels of electrical performance not possible with centralized architectures.

2.3.3.2 Allows use of Standard Modules

The usage of standardized power conversion hardware is one of the biggest advantages of decentralized architectures. Compared to the custom designs associated with centralized approaches, standard power modules offer lower development cost, faster time-to-market, faster qualification, higher reliability, more flexibility, significantly lower technical risk, and very competitive hardware costs. These advantages are so pronounced that we have included a complete chapter to discuss them in more detail.

2.3.3.3 Automated Assembly Process

On-board DC/DC power modules or BMPS are small and light enough to be assembled with automated assembly equipment, eliminating the manual labor traditionally associated with power converter installation. This results in significant cost savings as well as more reliable and dependable interconnections. BMPS are now available in SMT versions so that mixed packaging implementations are no longer required. It is now possible to achieve automated SMT manufacturing compatibility with BMPS up to 75 W.

2.3.3.4 Better Back panel Utilization

For rack type systems, where circuit boards are plugged into a back panel, the decentralized approach results in a significant advantage. Rather than distributing low voltages such as 3 V or 5 V at high current, a higher voltage such as 48 V is distributed. This results in reduction in back panel currents by a factor of 10 or more, and requires much less copper being allocated to the power function. The saved back panel area capacity can then be used for signal trace distribution.

2.3.3.5 Better Connector Utilization

Applying the same reasoning as above, the currents through the connector pins between the back panel and circuit boards are reduced by about a factor of 10. This means either that more pins are available for signals, or that a smaller connector can be used with resultant cost savings. The increased popularity of decentralized power architectures has resulted in the availability of standardized connector systems specially designed for reliable plugging of intermediate bus voltages.

2.3.3.6 Distributed Heat Load

Rather than concentrating power converters and their resulting power dissipation at one location in the system, decentralized power tends to diffuse it throughout the system. This can reduce cooling air requirements or in some cases allow free convection cooling with no need for fans or blowers. The result is higher reliability. The cooling requirements and interfaces of BMPS are well understood and documented. This makes it relatively easy for the power system designer to achieve a reliable and conservative system thermal design without the need for specialized hardware.

2.3.3.7 Ease of Battery Backup

More and more systems in the Information Technology and Industrial arenas are now recognizing the advantages of having a battery supported bus voltage similar to the approach traditionally used in the Telecom market. To achieve the benefits of operating through temporary loss of the AC power line, many approaches have been used, including motor generator sets and UPS systems. The use of a battery to support an intermediate bus voltage, such as shown in several examples here, provides these same benefits with levels of reliability and cost far superior to UPS implementations. This approach fits perfectly with decentralized power architectures.

2.3.3.8 Ease of Regulatory Qualifications

Distribution of an isolated SELV intermediate voltage greatly simplifies regulatory qualification, as does the usage of standard BMPS that have been granted agency safety approvals at a module level. This approach eliminates one of the major schedule roadblocks that often occur with conventional customized centralized architectures – the need for last minute safety approval of custom power converter designs.

2.3.3.9 Eliminate Problems of Multi-output Converters

Centralized architectures often require the use multi-output power converters. These converters are more difficult to successfully design than dedicated single output power converters. There are often undesired interactions between the outputs, such as cross regulation, noise coupling and dynamic response problems. Changes in the requirements in any one voltage level forces the entire power supply to be redesigned and possibly re-qualified. Decentralized architectures implemented with distributed power modules eliminate these kinds of problems entirely.

2.3.3.10 Enhanced Reliability

With older technology, replication of DC/DC converters in decentralized architectures would result in unacceptable reliability due to the summation of their individual failure rates. The newer BMPS now available offer extremely high levels of reliability, much more than can be achieved with larger conventional power converters. This is due, in part, to the high levels of integration and simplicity that can now be achieved along with the availability of specialized components. The latest BMPS offer failure rates over an order of magnitude lower than those of just a few years ago. Because of the importance of reliability in today’s system design, we have included a dedicated chapter on reliability. The chapter on total cost of ownership also instructive in terms of understanding the impact of reliability on cost.

2.3.3.11 Enhanced Failure Isolation Capability

The more decentralized the power system, the easier the power failure diagnosis and isolation becomes. This is due to the close association between power components and circuit functions in Power per Function and Power per Board systems. The spares stocking and field replacement also become easier as the power architecture becomes more decentralized and the BMPS become smaller and more granular. In the Power per Board implementation, DC/DC power modules do not need to be stocked at all as a repair part as they are automatically replaced as a part of the load board.

2.3.3.12 Fault Tolerance

Decentralized architectures lend themselves naturally to providing redundancy of function. Power per Board, for example, allows each board to be completely independent from a functional point of view. Failure of a DC/DC converter will only affect one board, and failure of the electronics on any board (such as a short circuit) will only affect one power converter. This results in dramatic increases in availability due to decreased propagation of failures between system sub-assemblies. It is possible for much of the system to remain up and running in spite of single point failures in either the power or load circuitry.

2.3.3.13 Flexibility for Upgrades and Features

One of the design goals of many systems is flexibility with regard to its size and performance options. For example, the manufacturer may want to be able to sell an “entry level” system and then later upgrade it with additional capability in terms of more features or enhanced processing power. Sometimes the end user rather than the manufacturer of the product is responsible for this upgrade activity. Ideally, the full range of systems should be accommodated by one basic power system design. These goals can be easily achieved by using decentralized power architectures with standard BMPS. The DC power required to operate the new circuitry can be added as part of the upgrade. Also, the base product design is not held up waiting for definition of all possible feature mixes. Power per board is the most flexible in this regard. Very significant cost and schedule enhancements can ensue.

2.3.3.14 Live Insertion / Hot Plugging

The maintenance and repair philosophy for high availability systems usually requires “live insertion” or “hot plugging” of sub-assemblies. Including the final stage of power conversion on the load assemblies, as in “Power per Board”, greatly simplifies this operation. The intermediate bus voltage is sufficiently high so that the current levels through the connector are modest. The intermediate voltage is also only loosely regulated and can withstand a greater voltage deviation during the plugging activity than would be possible with distribution of the final circuit operating voltage through the connector. The recent availability of “hot plug controller” ICs has also simplified the design of such systems. These products are specifically designed to allow the implementation of decentralized power systems demanding live insertion of the load cards.

2.3.3.15 Low Cost Entry Systems

With centralized power, the base product contains enough power capacity to power a fully configured system. This imposes a cost penalty on the low end user, and makes the system appear to be less attractive from a cost point of view. With decentralized power, the low end user gets the lowest possible cost of power, and pays for additional capability incrementally as features are added.

2.3.3.16 Lower Total Cost of Ownership

There has recently been more awareness of the total cost of a power system over the lifetime of the end product. These costs include the areas of product development, hardware procurement of power system components and system field support. The reliability of BMPS has a strong influence on the field support costs and consequently on the total cost of ownership. This topic is explored in some detail in the chapter on total cost of ownership. The high reliability of today’s standard BMPS results in dramatic reductions in the cost of ownership for decentralized power architectures.

2.3.3.17 Reduced Time-to-Market

Decentralized power offers a very significant advantage during the system development process. It is no longer necessary to wait for the complete definition of the power requirements for the system before beginning the design of the power system and its component converters.. Each function or each board can be characterized as it is developed, and appropriate standard converter modules selected. Modular front-end AC/DC converter systems and packaging approaches can be selected with the knowledge that the final configuration can be decided upon later in the system design process. Long lead times and constant redesign for power system development become a thing of the past.

2.3.3.18 Simpler DC Distribution

The Power per Board approach essentially eliminates low voltage DC distribution, except for the easy to implement on-board low current distribution on each circuit board. Wire harness assemblies and bus bars are eliminated. The need for remote sensing and its associated reliability and diagnostic impacts is eliminated. The intermediate voltage distribution tends to be very non-critical and inexpensive due to the DC/DC converter regulation that occurs later in the system.

2.3.4 ElectricalDesign

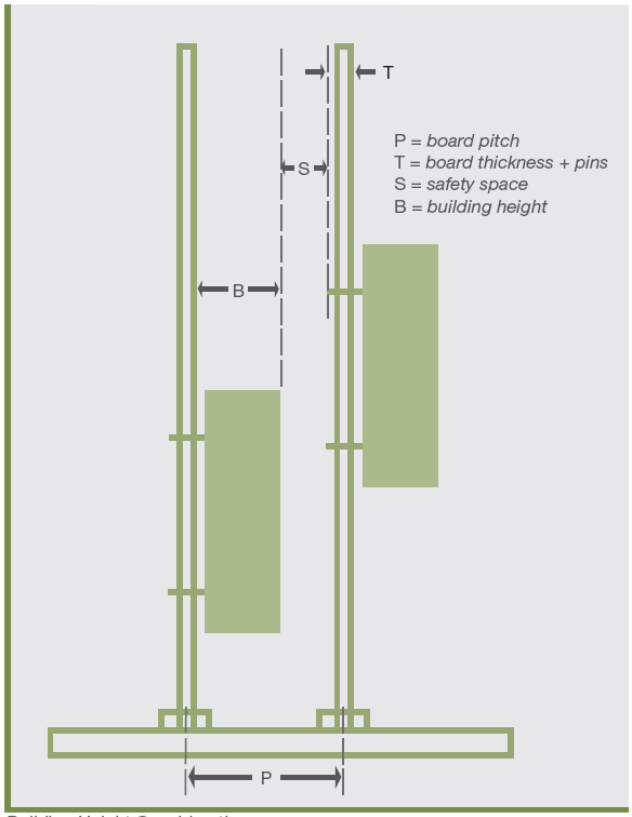
The power system designer's task is to select and apply standard BMPS in order to implement a power system that will provide the desired electrical and thermal performance as well as meet the system needs in terms of cost and reliability. A very important aspect of this overall objective is the electrical design, which consists of determining the required module specifications from the system electrical requirements and designing the electrical interfaces between the module(s) and the remainder of the system. An overview of the system electrical design process will be presented here.

Perhaps the most fundamental electrical design task is determining the DC voltage and current requirements for the system and translating them into appropriate ratings for the BMPS. We will investigate methodologies for accomplishing this and examine some of the trade-offs inherent in selecting module current ratings. Another area that is key to the success of the system is load partitioning. We will look at some partitioning strategies and see how they affect the BMPS selection. Power DC distribution and decoupling is much easier and simpler to design with decentralized power architectures, but still is an important component of the overall product design. We will address the requirements for decoupling and establish some guidelines for implementation. Several aspects of fault protection will be addressed and recommendations given for simple filtering and fusing which can add considerably to the ruggedness and robustness of the system. Paralleling of DC/DC converters will be discussed, along with the merits and disadvantages of using this approach. Finally, DC/DC converter controls and diagnostics will be considered.

2.3.4.1 Converter Power Sizing

The first task that a power system designer must undertake is to determine the power demands of the system. The mixture of circuit families used to implement the design usually defines the needed operating voltages. The designer's focus here is to minimize the number of unique voltages required. Additional voltage levels can add cost, complexity, the possibility of interaction, more difficult diagnostics, and reliability impacts. Once the minimal set of operating voltages has been decided upon, the next step is to determine the current demand at each of the DC operating voltages. This is often done in two stages – first estimation and then measurement.

Early in the system design process, even prototype hardware does not exist. Yet it is important at this stage to do a preliminary power system design so that the feasibility of the resulting power system concept can be proven. This first iteration of power design is accomplished by using estimates of the expected current demands for each voltage level. For newly designed custom discrete circuitry, the current estimate must be obtained either from a specification for the circuit function or from the judgment of the circuit designer. These types of estimates can vary widely in accuracy. Although it cannot be guaranteed, most designers tend toward conservatism in their estimates. It is not uncommon to find initial estimates that overstate the current demand by factors of 2 to 3. The best way for the power system designer to probe or challenge these estimates is to ask for the assumptions and operating conditions for



Building Height Considerations

Figure 2.3.7.2

If allowances are made for tolerances, pin extension through the board, board thickness, and safety spacing, the module building height must be as small as 12mm in many cases. Figure 2.3.7.2 depicts some of the considerations that determine the allowable module building height for pinned converters. SMD converters offer the advantage of no pin protrusion through the board and, in the case of planar open frame designs, lower module height. As a consequence, these newer designs are more flexible when applied to systems with small board-to-board pitch.

In summary, the best BMPS design and package is one that is optimized to the user's building practice. A high power DC/DC converter designed to be used in a power per shelf architecture with an attached heatsink will be packaged considerably differently than a low power SMD converter used in s power per board application. Products should be available to allow compatibility with either through hole or SMD assembly processes. Low building height is becoming very critical for many applications.

2.3.8 Reliability

Reliability and availability is one of the key selling points for electronic equipment. This was always true in the telecom and military marketplaces, but it is now also a priority in the datacom, industrial and even consumer markets.

2.3.8.1 Introduction

Present day analog and digital ICs, when properly applied, are very reliable, and most equipment manufacturers use similar components from many of the same suppliers. Consequently, the power system for the equipment often is one of the few ways for the manufacturer to differentiate the product

from those of its competitors. Because of their design complexity, component stress levels and variation in power dissipated, today's high power density converters can vary widely in reliability. Some of them will be the most unreliable part of a system. The better ones are capable of demonstrating truly astounding levels of reliability and availability. In this treatment of reliability, we will define some terms and concepts, show examples of how to use the concepts, and examine various ways of predicting and measuring BMPS reliability. We will also address the design and procurement practices available to the power system designer and see how they affect the overall reliability level of the product. Finally, we will consider the concept of power converter lifetime or wear-out and see how it relates to failure rate and MTBF.

2.3.8.2 Definitions and Concepts

The most fundamental concept in electronic reliability theory is the so-called 'bathtub' curve that depicts how the failure rate of a component (or assembly of multiple components) varies as a function of time. This curve is shown in a general way in figure 2.3.8.1. The values on both ordinates will vary widely depending upon the types of components and systems that are being evaluated, and we will address some appropriate typical numbers for BMPS and systems later in this chapter. For now we will discuss the effects shown on the curve in a qualitative way.

The area at the beginning of the curve is called the infant mortality period. This time period represents the first few hours (typically less than 200) of a component's or product's life. The failure rate is generally higher during this period due to fallout of manufacturing defects and marginal components. As we will see, there are often actions taken by manufacturers on the component, sub-assembly and product levels to prevent these failures from occurring after the product is in the customer's hands. The most common technique for achieving this end is a 'burn-in' process.

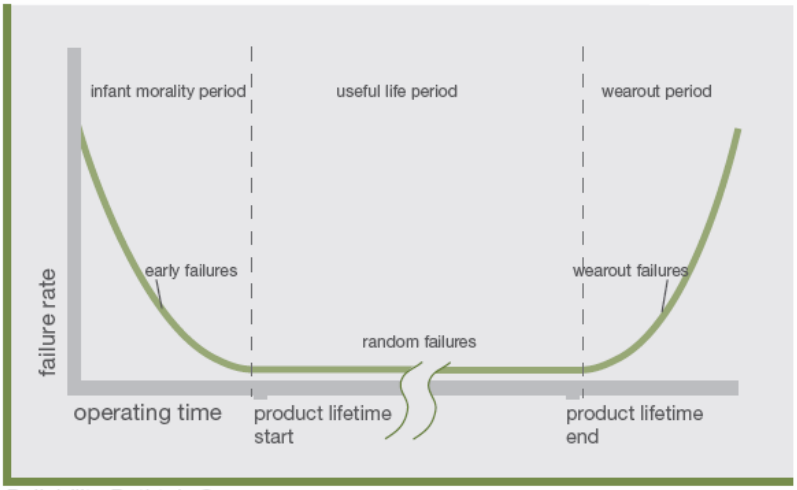


Figure 2.3.8.1

At the other end of the time spectrum is the area labeled "wearout period". After extremely long periods of time some electronic components begin to fail due to known long-term wearout mechanisms. Some examples are certain types of electrolytic capacitors, batteries and fan motors. For other components the longterm failure mechanisms either do not exist or are not yet known. In any case a good product design will have no known wearout mechanisms occurring before the expected product lifetime ends, which is normally determined by obsolescence or economic replacement intervals. With today's better BMPS offerings this goal can be easily achieved.

The period between the infant mortality period and the wearout period, referred to as the "useful life" period, is much more interesting and relevant. This period is of significantly greater duration than either of

the other time intervals and is the time during which the equipment or component is expected to operate in a reliable fashion. As can be noted from figure 2.4.5.1, there are two important characteristics of the failure rate during the useful life period:

- The failure rate is constant
- The failure rate is low

Formatted: Bullets and Numbering

This low and constant failure rate is due to random component failures, and is influenced by operational stress and temperature conditions. We will be discussing this type of failure rate in great detail since it is what determines the real-world reliability of all electronic products.

As the name implies, the failure rate has the units of failures per unit of time. We designate failure rate with the symbol **λ**. Therefore a low value of ë implies a low failure rate and a high reliability. **λ** is referred to as the "intrinsic failure rate", or IFR. This relationship is expressed mathematically by using the exponential reliability function that defines the probability of a component operating after time t as:

$R(t) = e^{-\lambda tt}$

where: **λ** is the constant failure rate.

Using this expression, what is the probability of a capacitor operating after 300,000 hours if its failure rate is 5 × 10-7 failures per hour?

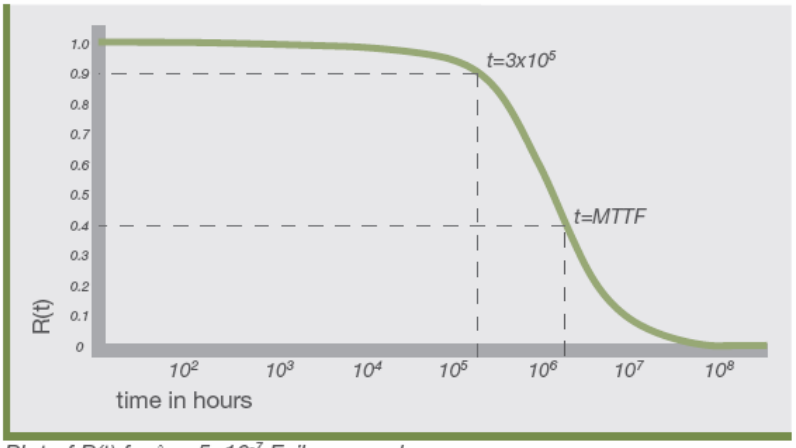
with =**λ** 5×10^{-7} and t = 3 × 105
λ t = (5 × 10-7)(3 × 105) = 0.15
$R(t) = e^{-0.15} = 0.861$

and the probability of no failure after 300,000 hours is 86%.

Similarly, we can calculate R(t) as a function of t with the result as shown in figure 2.3.8.2. Note that the probability of failure remains very low until the operating time becomes quite large (105 hours) and that the probability of failure becomes very large when the operating time is above 107 hours. If the component sample size is large, most of the units failing will fail within this period of time (see also section "Failure Rate, MTBF, and Lifetime"). There is sometimes confusion when using failure rates due to the lack of standardization of units for ë. If highly reliable components are being considered expressing ë in units of failures per hour results in very small numbers. Because of the awkwardness of using failures per hour, there are other units used in practice in various corporations. Some of the more commonly used units are:

- Failures per million hours
- % failures per thousand hours

Failures per billion hours, referred to as "FIT", an acronym for "Failures in Time".

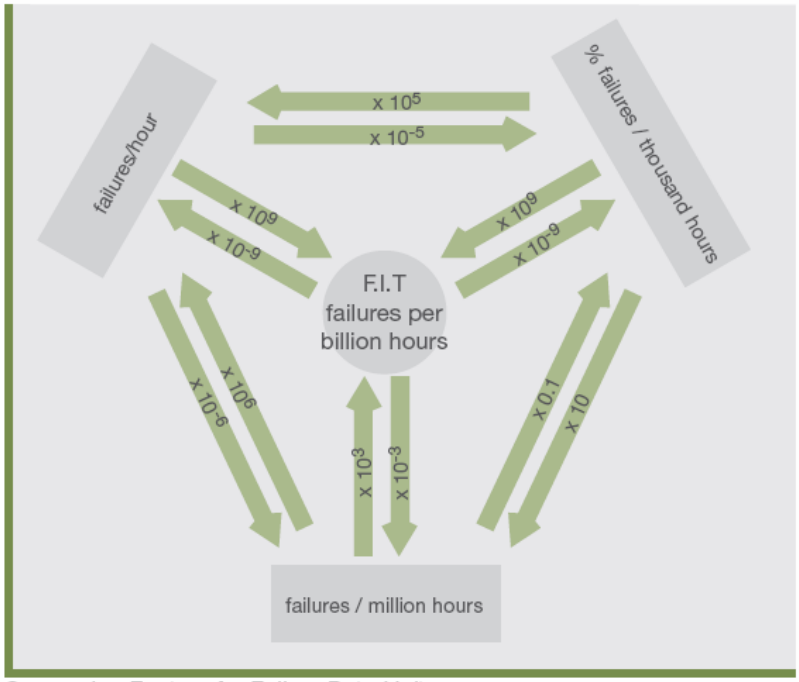


Plot of R(t) for $\lambda = 5\times10^{-7}$ Failures per hour

Figure 2.3.8.2

All of the above are equally valid ways to represent the IFR. With the increasing levels of reliability and the corresponding reduction in the size of ë for today's electronics it is recommended that the FIT terminology be used. This will result in numbers that are easier to record and manage. Failure rates expressed in any of these units can be converted to any other unit by using the conversion factors shown in figure 2.3.8.3.

Given failure rates for individual components, the failure rate of an assembly of these components is obtained simply by summing the individual failure rates. This approach assumes that the failure of any component results in failure of the assembly. This assumption, in practice, is close enough to reality that the resulting mathematical simplicity is well worth the very slight difference in the reliability calculation. Also IFR calculations are based on many assumptions about the components and their operating conditions and the results are accurate to at best ± 10%. The effect of the above assumption will normally be less than this.



Conversion Factors for Failure Rate Units

Figure 2.3.8.3

We will now calculate the failure rate for an assembly composed of several components. The overall IFR is the summation of all the individual component failure rates. Normally there are many components with the same approximate failure rate (i.e. – all thick film resistors of a given power rating), so a commonly used expression to calculate the IFR of an assembly is:

$IFR = \boldsymbol{\lambda}_A = n_1 \boldsymbol{\lambda}_1 + n_2 \boldsymbol{\lambda}_2 + n_3 \boldsymbol{\lambda}_3 + ... + n_i \boldsymbol{\lambda}_i$

where: $\boldsymbol{\lambda}_A$ = IFR of Assembly
n_i = Number of component type i
$\boldsymbol{\lambda}_i$ = IFR of component type i

Using this approach we will calculate the assembly IFR of a multi-component assembly as follows:

Type of Component	**Number Used**	**Component IFR (FIT)**	**S IF IFRR (FIT)**
Resistors	10	100	1000
Capacitors	5	500	2500
Transformer	1	50	50
Power Transformer	2	1000	2000
Total			5550

The assembly failure rate is 5550 FIT or 5.55×10^{-6} Failures/h

Even though we cannot predict exactly when each component will fail, if there are a large number of components operating under the same conditions we can predict the average or mean time that a

component will operate before failing. In the case of figure 11.2, for example, most failures occur between 105 and 107 hours, and we would expect the average time to failure to be somewhere within this range. Solving the reliability function for the mean, we find that the mean time to failure occurs when t has a value of 1/ë. The mean time to failure is often abbreviated as MTTF, and the units are hours to failure. MTTF s can be found by taking the inverse of the IFR, or ë. Some MTTF s from our previous examples are:

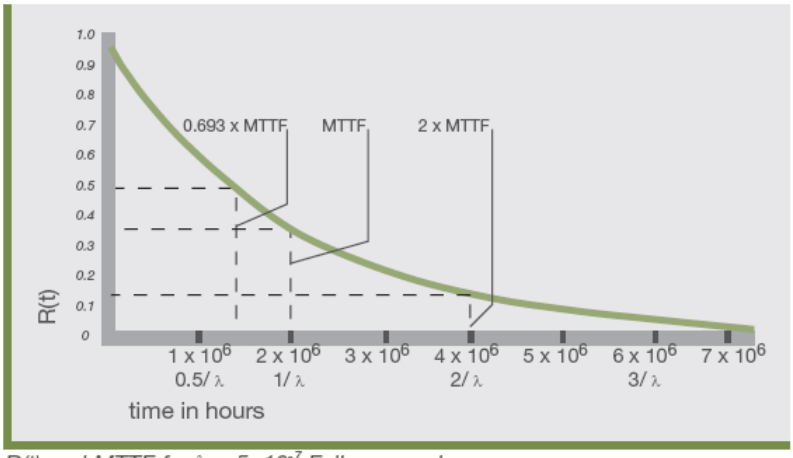
Example	**λ**	**MTTF (hrs)**
Capacitor	5 x 10-7	2,000,000
Assembly	5.55 x 10-6	180,180

Another term commonly used in reliability analysis is MTBF, or Mean Time Between Failures. MTBF is found by using the MTTF and adjusting the result for the length of time required to replace failing units and restore operation to the end product. Present day technology, with very low failure rates and efficient field service practices, normally negates the need to adjust for restoration time as it tends to be insignificant compared to the MTTF. Consequently, except for very special situations, we can define MTBF to be essentially equal to MTTF. Thus:

MTTF = 1 /**λ** ≈ MTBF

Even though MTTF is mathematically the more correct terminology for items such as components and BMPS that are not repaired in the field, MTBF is more commonly used than MTTF and we will sometimes use it here. Mostly, however, we will use IFRs, as they are easier to work with mathematically and tend to avoid the confusion that sometimes occurs between MTBF and product lifetime.

If we plot the same relationship as shown in figure 2.3.8.2, but this time on a linear scale centered on the MTTF, we obtain the result shown in figure 2.3.8.4. This shows us that, for a large sample size, 37% of the units will be operational after time MTTF, and that 50% of the units will be operational after time 0.69 × MTTF, if the IFR remains constant over this time.



R(t) and MTTF for λ = 5×10^-7 Failures per hour

Figure 2.3.8.4

2.3.8.3 Reliability Prediction and Measurement Techniques

We now know how to express and use failure rates and how to convert them to MTBFs. We have not, however, addressed the source of the IFR values we used in the preceding section. There are two main categories of IFR determination - prediction and measurement. Prediction techniques are used to

estimate the IFR of an assembly before it can be tested. Measurement techniques are used when access to actual operational hardware data exists. In this section, we will discuss the most commonly used IFR prediction and measurement techniques:

Prediction

Military handbook
Bellcore/Telcordia
Supplier database
Field history of previous designs

Measurement

Field history
Accelerated life testing

As we will see later, measurement techniques are very time intensive, often requiring months or years of effort to arrive at meaningful results. Product development time-to-market considerations typically do not allow for extensive measurement of reliability during the development period. In spite of this, we must have a way to determine the reliability of new designs. To solve this problem reliability prediction techniques have been developed.

The most widely known and used prediction method is the so-called 'Mil-Handbook' approach. Because of the military's concern with the reliability of its electronic products, they developed a very detailed methodology for calculating predicted reliability. This methodology is documented in a handbook referred to as 'MIL-HDBK-217'. As of mid 2001, this document is at revision level F, notice 2. The MIL-HDBK-217 approach is basically identical to the technique we used in section "Definitions and Concepts" to derive the IFR for an assembly from the summed IFRs of its constituent components. The only difference is that the MIL-HDBK-217 technique modifies the base failure rate of each component in an attempt to account for the quality of the component and the operational conditions for the component. In general, each component failure rate is modified for the following parameters:

- Component quality and sourcing
- Operating environment
- Circuit density
- Temperature

The modified component failure rates are then summed to arrive at the predicted IFR for the entire assembly. This approach has merit as a concept, but in practice has several shortcomings that have limited its direct usage to military systems. Some of the problems with applying the MIL-HDBK-217 method to nonmilitary systems are:

- The MIL-HDBK is dependent upon a database of component types and their corresponding failure rates. This database takes time to be generated and focuses on the component types developed for military systems. As a consequence most newer commercial technologies and components are not available in the database. Reliance on the MIL-HDBK for reliability prediction results in designs lacking
  innovation and no usage of newer components with better performance and reliability
- The MIL-HDBK imposes a very harsh reliability penalty to non-military components. In reality, many of
  the better commercial components come down the same manufacturing line at the component vendor as the equivalent military part and are physically identical. The only difference is the extra documentation and extended testing that the military part is exposed to. Several independent tests have shown that, with intelligent procurement, commercial parts with reliability performance equal to military equivalents can be obtained
- The MIL-HDBK assigns failure rates to some components that are not consistent with their actual performance. For example, transformers and magnetic devices have a very low actual failure rate but the MIL-HDBK IFR prediction is very high. An even better example is integrated circuits. We have all experienced the growth in reliability of systems configured with a smaller number of ICs replacing

large quantities of discrete components. Yet the MIL-HDBK assigns very high IFR values to ICs, and penalizes integrated solutions. The result can be that designing to minimize MIL-HDBK IFR values can sometimes result in a less reliable product

In cases where MIL-HDBK predictions have been compared with actual field performance, it has been found that for power converter assemblies the IFR predicted by MIL-HDBK techniques is in the range of 3 to 10 times higher than actual field failure rates. Another commonly used prediction technique is based upon Bellcore reliability test methodology. Bellcore (Bell Communications Research) was a spin-off from AT&T and is the R&D organization of the Bell operating companies in the US. Bellcore now supports and continues development of a reliability prediction methodology originally developed by AT&T Bell Labs in the mid 1980s. Bellcore is now transitioning to the name “Telcordia” for at least a portion of their operations. The document that defines their reliability prediction technique is TR-332 “Reliability Prediction Procedure for Electronic Equipment”. This document was at “issue 6” revision in mid 2001.

The Bellcore/Telcordia methodology is conceptually very similar to the MIL-HDBK approach, but is optimized for telecom systems. It includes component types used in telecom systems that are not covered by the MIL-HDBK system. It also includes provisions for the usage of burn-in and field reliability data and is therefore much more flexible in terms of incorporation of historical data in addition to theoretical predictions. Bellcore/Telcordia prediction methods are widely accepted in the US and are now gaining more acceptance worldwide. The failure rate prediction results using Bellcore/Telcordia techniques are typically lower (and therefore closer to actual field performance) than those resulting from MIL-HDBK procedures.

In an attempt to retain the very valid concepts and methodologies of the MIL-HDBK and Bellcore/Telcordia approaches, but remove the shortcomings of the component database, many power supply manufacturers utilize their own database of component IFR performance. These suppliers are usually large corporations that have the benefit of doing some of their own component development, have access to failure analysis data from field failures, or have accumulated significant experience with manufacturing very large quantities of power supplies. These ‘supplier databases’ contain up-to-date information on the types of components actually used by the supplier. Variation in IFR between component vendors is tracked. The resulting information is more accurate than the MIL-HDBK data and represents a very powerful and valuable competitive advantage for the BMPS supplier. Of the prediction methods presently available, this is perhaps the most accurate and consistent predictor of operational performance.

Another predictive approach that can be used by a BMPS manufacturer is to estimate the IFR of a BMPS based on the assembly level field history of similar products. This can be a useful and easy to apply technique if the new design is similar to an existing design. For example, if only the output voltage of a converter is changed, it is reasonable to assume that its failure rate will be very similar to other previous converters using the same topology and components. This technique is less useful for prediction of IFR performance of designs that are significantly different from past designs.

It should be noted that field history is not easy to obtain. A big percentage of failed units are sometimes discarded and replaced without notifying the power supply manufacturer, so that returns to the manufacturer are only a subset of the total field failures. The best field history information exists within vertically integrated companies that not only manufacture BMPS but also use these converters within their own products. These companies can tap into the product repair records and be aware of all field incidents involving the BMPS.

We will now address methodologies for measuring reliability as opposed to predicting it. By far the most accurate method of reliability measurement is analysis of actual field data. It measures large quantities of units under actual user conditions. Probably the most difficult aspect of collecting field history is to accurately assess the number of operating hours on each BMPS. For telecom and some datacom applications that operate close to continuously, the operating hours can be obtained fairly easily. For other types of equipment such as personal computers and consumer electronics, it is much more difficult to assess operational time. With good data for number of failures and number of operating hours, it is an easy calculation to obtain the overall IFR for the BMPS assembly. If the BMPS are returned to the manufacturer for failure analysis, failures can be traced back to individual components and component level IFR data developed. Even though the field history method is the most accurate, it has one very big

disadvantage – the data isn't available for months or years after the product is released. It is of no use in developing new designs or in predicting IFRs for newly introduced equipment. To remedy this major shortcoming, the accelerated life testing method of reliability measurement was developed.

Life testing consists of accumulating a significant number of operating hours on a product in a reasonable length of time by operating multiple units at the same time. Since it is the IFR, or random failure rate, that is desired, it is important to use units that have passed the burn-in test and have survived past the infant mortality period. Life testing is a measurement technique since it uses a sample of actual product rather than just analytical calculations. For inexpensive products or assemblies with fairly large failure rates, practical life tests can be done without acceleration. For example, if a DC/DC converter has an IFR of 1×10^{-4} failures/h and a quantity of 100 of these converters are operated continuously for a period of 30 days (720 hours), the expected number of failures would be:

(100) (1×10^{-4} fails/h) (720 h) = 7.2 Failures

The actual IFR would then be calculated based on the actual number of failures occurring within the 30 day test period. Here is a case where an unaccelerated life test is fairly economical and time efficient. This is not the case for present day power module technology that can exhibit IFRs in the range of 300 FIT. Using this number, the expected number of failures for the above test would be:

(100) (300×10^{-9} fails/h) (720 h) = 0.022 Failures

This number is much too small to be useful for a valid life test. In fact, to obtain 10 expected failures, one of the following test plans would be required:

- 100 units for 333,333 hours (38.1 years)
- 46,296 units for 30 days

The first alternative is unacceptable in terms of time, and the second unacceptable from a cost and implementation point of view. It is because of these problems that the concept of accelerated life testing was developed. Accelerated life testing essentially simulates very long test times by means of increasing the stress applied to the units and using a more reasonable and practical test time.

The stress level is increased by operating the BMPS at a temperature that is elevated relative to the normal operating ambient temperature. The greater the ratio of the test temperature to the operating temperature, the greater the acceleration factor. The acceleration factor also is affected by a variable called the activation energy. The activation energy varies from component type to component type because the failure mechanisms differ greatly, but for power converter life testing an average value in the range of 0.6 eV to 0.8 eV is commonly used. Temperature ratios and the activation energy is used in the Arrhenius equation to determine the temperature acceleration factor. It is tempting to use very large acceleration factors to reduce the length or sample size of life tests, but large acceleration factors increase the uncertainty of the resulting data. In order to obtain data that will be widely accepted as valid, it is best to limit the acceleration factor to 15 or less.

If the life test of the 300 FIT converter described above is redesigned as an accelerated life test with two expected failures, an acceleration factor of 10, and 200 units under test, the required test time would be in the order of 3000 to 4000 hours or 5 months. This is certainly a more reasonable test in terms of both time and expense than the available alternatives without acceleration.

2.3.8.4 Failure Rate, MTBF, and Lifetime

As we have seen previously, MTBF is approximately the inverse of $\boldsymbol{\lambda}$, the failure rate. A low failure rate implies a long MTBF. These are both valid statements, mathematically and in practice. We have used failure rate rather than MTBF in most of this text for two reasons. First, failure rates can be directly added when computing cumulative failure rates for assemblies with multiple parts, while MTBFs need to be converted to failure rates, added and then converted back again. Secondly, MTBF is a concept that sometimes gets misunderstood and consequently misused.

MTBF is sometimes confused with lifetime even though they are the result of completely different failure mechanisms. MTTF and MTBF are statistical measures determined by random failures that occur during the useful life period of the bathtub curve (figure 11.1). Component lifetime is driven by wearout mechanisms that are often very different in nature and occur in the wearout period of the bathtub curve. The misunderstanding centers around the very large MTBF values calculated from the IFRs of today's very reliable electronics.

Let us look at some numbers for power supplies. These can be considered typical reliability indicators for the best available power supplies for the respective years.

Year	Converter	IFR (FIT)	MTBF (h)	Telecom * MTBF (yr)	Office ** MTBF (yr)
1975	AC/DC Early Technology	50,000	20,000	2.3	9.6
1985	AC/DC Better Technology	10,000	100,000	11.4	48.1
2000	Board Mounted DC/DC Power Module	200	5,000,000	571	2,404
*	Assumes Continuous Operation (8760 hours per year)				
**	Assumes 8 hours per day, 5 days per week, 52 weeks per year (2080 hours per year)				

The above analysis also assumes that the power-off failure rate is zero, which is not strictly true.

As the IFR has improved with time the MTBF calculation has resulted in some very impressive numbers. The difference between MTBF and Lifetime can then be shown by the following example:

The reliability function, R(t) =e-□t, can be used to determine the probability of operation after t = MTBF

$R(t=MTBF) = e^{-(MTBF/MTBF)} = e^{-1} = 0.368$

This means that for a large population of the board mounted DC/DC converters, 36.8% will survive the first 571 years of operation if the IFR remains constant over this time. It does not mean that on average a DC/DC converter will operate for 571 years.

However, it would be unrealistic for the IFR to remain constant for that long. Components that exhibit wear-out mechanisms determine the useful lifetime of the DC/DC converter and other power supplies. Some wear-out mechanisms are:

- Long term chemical interactions between materials
- Shock and vibration effects on components, wire bonds, solder joints
- Temperature cycling effects such as stresses due to thermal coefficient of expansion mismatches
- Long term penetration of moisture into device packages

One component type whose lifetime has been suspect is electrolytic capacitors. Recent research has shown that the lifetime is highly dependent upon the type and quality level of the capacitor and the circuit application and the stress levels imposed on the capacitor. Specifically, solid tantalum capacitors have demonstrated service lives in excess of 20 years if properly derated and not exposed to high dV/dt stresses. The output filter of a DC/DC converter is an application that meets these requirements. The dV/dt applied to the capacitor is limited by the converter ramp-up circuit and also by the other elements in the output filter. Also, the converter limits the maximum energy that can be applied to the capacitor. If a good quality capacitor with a rated voltage of greater than 2 times the converter output is selected, extremely reliable and long life operation is achieved. It should be noted that rated voltage changes with temperature.

It is important to realize that the input filter of a DC/DC converter does not meet the above conditions. Very high values of dV/dt with extremely high energy levels can be imposed on the capacitor by transients on the input voltage as described in chapter 8. For this reason, the reliability and lifetime of DC/DC converters utilizing an electrolytic capacitor as part of the input filter should be questioned. The probability of the above type of problems can be minimized and the projected converter lifetime maximized by selecting the proper converter. Below are some guidelines for making this selection.

Minimize

- Number of different materials used
- Number of process chemicals used

Maximize

- Usage of stable & inert materials
- Silicon integration
- Thermal performance of passive components by mechanical integration
- Knowledge of components
- Manufacturing process controls, including cleaning

To summarize, maximum lifetime is achieved when a well understood and proven design is manufactured by a supplier who places emphasis on a controlled and clean manufacturing process. Successful designs tend to be highly integrated and manufactured in a manner that resembles process lines in an integrated circuit facility. The better suppliers will be proud of what is inside their product and share with you the criteria they use for component vendor selection. They will also offer tours of their process lines so that you may see the care and controls that are included in the manufacturing process.

A way to approach the issue of lifetime is to compare the operating lifetime of components and sub-assemblies that are determined by wearout mechanisms to the useful lifetimes for products that are driven by economic and marketing considerations. Below are some typical product lifetimes:

Product Type	**Lifetime (years)**
Personal Computer	5
Mainframe Computer	10
Telecom System	20

BMPS intended or use in telecom equipment are designed for product lifetimes exceeding 15-20 years. This is verified through extensive long term component testing and temperature cycling of the BMPS.

A realistic application of MTBF numbers for BMPS is in predicting the percentage of units that can be expected to survive to a given time. If the BMPS in the previous example has a useful life of 20 years, the percentage of units that will survive the useful lifetime is calculated by:

$R(20year) = e^{-(20/571)} = 0.966$

Therefore, 1 - 0.966 = 3.4% of these units will fail before wear-out occurs. Using the 200 FIT IFR, let us also calculate the expected number of failures per year experienced by the manufacturer of the office equipment assuming the following implementation:

Number of DC/DCs per product 3
Number of Products in field 10,000

Failures/yr = (200×10-9 fails/h)(2080 h/yr)(3)(10,000) = 12.5

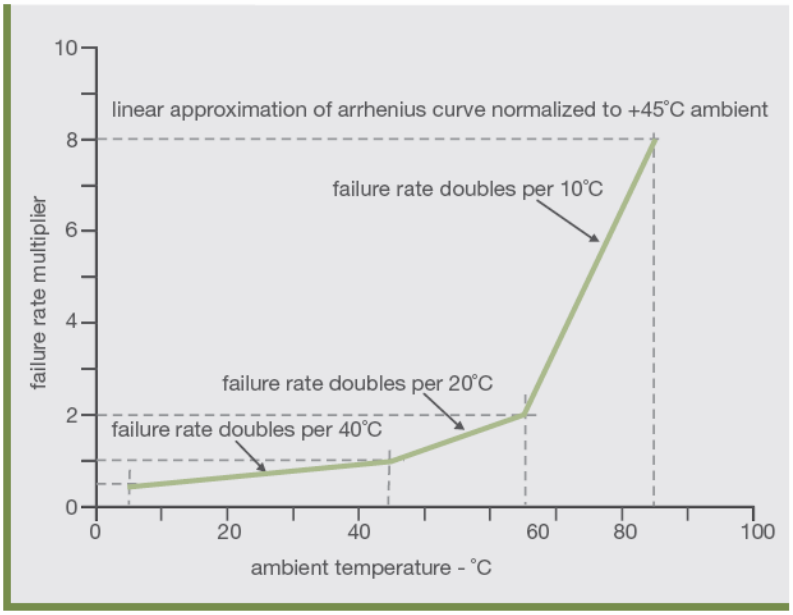
MTBF = 1/12.5 = 0.0801 yr = 29.2 days

For the 30,000 converters in the field, the manufacturer can expect failures at average intervals of 29 days, and should structure the field service strategy and spares stocking in accordance with this estimate.

2.3.8.5 Design Practices for Maximum Reliability

Manufacturers have made significant progress in enhancing the reliability of the available BMPS, with some of today's offerings being capable of failure rates as low as 200 to 400 FIT. In order to achieve this kind of performance within the product application, the user of these modules should be aware of the external factors that influence the BMPS reliability. Intelligent design of the power system can contribute greatly to system reliability by insuring that the stresses imposed on the BMPS are consistent with long life.

By far the single most important factor under the control of the power system designer is the temperature of the BMPS. When operated within the specified limits the modules will be safe and reliable, with all components below their maximum allowable operating temperatures. But as we saw in the section on accelerated life testing there is a definite relationship between operating temperature and expected reliability. The module user can take advantage of this fact and improve the system reliability to even greater levels by controlling the module temperature. The module reliability is predicated on an average ambient temperature of +40 to 45 °C. In applications with prolonged exposure to higher ambient temperatures the IFR will be degraded. If the average ambient is less than +45 °C, the failure rate can be even lower than the projected datasheet values (see figure 2.3.8.5). There are two main ways of achieving this end – derating the BMPS and controlling the ambient temperature.



Effect of T_A on Ericsson DC/DC Power Module Reliability

Figure 2.3.8.5

The thermal design of the BMPS and the failure rate prediction assume that it is operating at its maximum rated output power. If it is operating at less than full load, internal power dissipations will be less as will all the temperatures internal to the module. For the components inside the BMPS, reducing the load current will have the same effect as lowering the external ambient temperature – a lower temperature rise between ambient and the internal component temperature. Running a BMPS at half load, for example, will reduce internal power dissipation by half and the internal temperature rise will be half of the full load

value. This could result in component temperature decreases of up to 20°C, and substantially improved reliability. Even derating to 70 or 80% can result in very meaningful and measurable reliability enhancement.

Control of ambient temperature is equally powerful as a tool for reliability design. The lower the case temperature (for convection cooled BMPS) or the pin temperature (for conduction cooled BMPS), the better the reliability. In either case, lowering of the system's internal ambient temperature will enhance the reliability. If this is not possible, some of the techniques discussed in the thermal design chapter will be helpful in lowering the temperature at the module. Some of the possibilities are heat sinking, forced convection cooling, careful placement of BMPS in free convection systems, and thoughtful board layouts. The bottom line is:

Cooler BMPS = Better Reliability

The above hints will be very successful in controlling thermal stress to the BMPS. Electrical stresses should also be considered. The most common electrical stress that can degrade the BMPS reliability – or even cause immediate failure – is voltage transients on the input. BMPS are designed to operate over a wide range of DC input voltage to allow for convenient application to telecom systems. In real-world systems, there are often transients on the DC input bus that can exceed the DC static voltage limits. This transient activity can be the result of load switching in other parts of the system, fault conditions in the system or external to the system, or external influences such as lightning strikes, etc. The inductive elements of the system DC distribution network can contribute to making these transients even worse. System designers can prevent problems in this area by understanding the DC distribution system. The system should be modeled with equivalent resistive, inductive, and capacitive elements, and the effects of load switching and other system effects studied. If required, the internal BMPS transient suppression capability can be supplemented with additional components external to the BMPS. This topic is covered in greater detail in the chapter on power system electrical design.

2.3.8.6 Procurement Practices for Maximum Reliability

We have seen above how the power system designer can improve the reliability performance of the system by how he/she applies BMPS. Of equal importance to achieving the system reliability goals is selecting the proper BMPS and supplier. The design of the BMPS, the manufacturing process, and the supplier's testing process are all of critical importance and vary widely from supplier to supplier. The better manufacturers will have a detailed understanding of the reliability impacts of all aspects of their design and manufacturing environment and demonstrate a willingness to share this knowledge with their customers. Below are some of the criteria to explore when selecting a supplier for high reliability BMPS:

- Experience with application of its BMPS in actual high reliability systems
- Access to long-term field performance data for tracking of reliability
- Intensive knowledge of components, including database of actual failure rates as a function of stress for components used in their designs
- Design integrity – proven designs and well conceived new designs
- Conservative thermal design
- High baseplate or case temperature rating
- High efficiency
- Accelerated life testing of new designs
- Care in component vendor selection
- No electrolytic capacitors in input filter designs
- Simple designs with high levels of integration and low component count
- Hybrid-like packaging
- Thick film resistors rather than discrete
- High degree of automation in manufacturing process
- Tight manufacturing process controls
- Emphasis on process cleanliness
- 100% burn-in to deliver units with lowest possible failure rates
- Use of environmental stress testing to increase assurance of reliable long-term performance when exposed to temperature, humidity, shock, vibration, temperature cycling, power cycling, etc.

2.3.8.7 Examples of Power System Reliability Calculations

Now that we have explored some of the concepts of power system reliability, we will apply them to some examples, showing how the reliability assessments will help in making system architecture and logistics decisions.

Example 1 - Expected failures and spares strategy

A system is configured with distributed power modules on a power per function basis (each power module is mounted on its own PCB and supplies power to adjacent boards). There are a total of 12 identical power boards in the system, and each board assembly has a failure rate, I, of 500 FIT. The system is a telecom product and operates continuously. What is the expected number of power board failures per year for each system? How many spare boards should be stocked?

With continuous operation, there are 8760 operating hours per year. For the 12 units, the expected number of failures per year is given by:

(12) (500 × 10^{-9} fails/h) (8760 h) = 0.053 Failures

We find that the probability of a failure within the one year period is very small. Stocking one spare power board assembly should be sufficient.

Example 2 - Effect of power module failure rate on repair actions

We saw in the previous example how highly reliable BMPS can result in very reliable power systems with minimal exposure to field replacements. We will now expand upon this example. Assume that the product manufacturer has a total of 2000 of these systems in the field under warranty. What are the total yearly module replacements as a function of module reliability? Assume a range of reliability consistent with presently available BMPS (10,000 FIT to 200 FIT). For the 500 FIT unit, we obtain:

(2000) (12) (500 × 10^{-9} fails/h) (8760 h) = 105 units

Repeating this calculation for other values of **λ** we obtain the following result:

Power Module Failure Rate - I (FIT)	**Yearly Replacement**
10,000	2,102
5,000	1,051
2,000	420
1,000	210
500	105
200	42

The more reliable BMPS offer a very significant reduction in yearly replacements that will drastically decrease the costs for replacements and labor. Further, it will simplify the field service strategy and result in a much better reliability reputation for the manufacturer's products.

Example 3 - Comparison of power architectures

Consider a rack and shelf telecom system, where the designer can either use a 'power per shelf' concept or a 'power per board' approach. The shelf DC/DC would be a 100 W unit with a failure rate, IPS, of 1500 FIT. For the board mounted version, each board would contain a 25 W output DC/DC power module with a IPM of 500 FIT. See figure 2.3.8.6 for a sketch of each power architecture implementation. Each of the functions is identical and serves the end users. The electronics of each function has a IFU of 2500 FIT. It is desired that this be a high availability system, with the maximum number of functions operational at all times. Compare the two power architectures in terms of the total reliability per function.

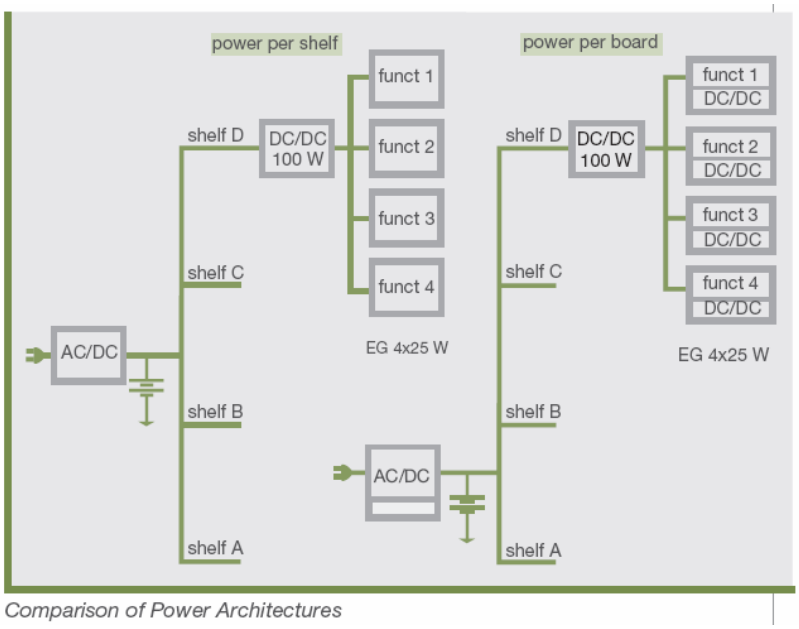


Figure 2.3.8.6

Since the front ends of both power systems (AC/DC and battery) are identical and have the same failure rates we can ignore the front ends and focus on the DC/DC conversion alternatives and the function boards. For the power per board approach, the total failure rate for the function is the sum of IFU and IPM, or 3000 FIT. For the power per shelf alternative, failure of either the DC/DC or the function board electronics results in failure of the function. Thus the total failure rate of any given function is the sum of IFU and IPS or 4000 FIT. We see that the reliability per function is higher with the board mounted power alternative.

There are additional considerations. In the power per shelf design, failure of the DC/DC converter results in loss of 4 functional units vs. only one unit for the power per board design. Furthermore, any power per board unit could be exchanged without interrupting the operation of the other functions. Thus, the availability advantages of the fully distributed approach are greater than the 1.33 times improvement in the individual functional element reliability.

2.3.9 Cost Analysis

Cost is one of the most important issues in equipment design. It is invariably one of the first three criteria on the list of priorities when selecting a power supplier. In spite of this very valid focus on cost there has been very little information published in the industry on cost analysis techniques for power systems. In this chapter we introduce methodologies for making informed decisions when comparing the costs of alternative power system implementations.

2.3.9.1 Introduction

We will first address the cost implications of reliability. For the past several years reliability has been identified as a very important issue in power system design. Most of the focus has been on issues such as system availability and customer satisfaction, with little attention on how reliability affects the bottom line costs of the system manufacturer. We will explore how BMPS reliability affects total lifetime system costs and find that the reliability performance can have a profound effect on total system cost for systems of even moderate size.

2.4.3 Power Converter Topologies

Converter topology is a much debated topic between converter designers and researchers who are trying to optimize device-level characteristics, component stresses and hardware costs. There are hundreds of different topologies and variations that can be used to implement DC/DC converters in the power range of 5 to 300 W, so it obviously is not practical to cover them all in this limited space. Rather a high-level overview will be given.

2.4.3.1 Introduction

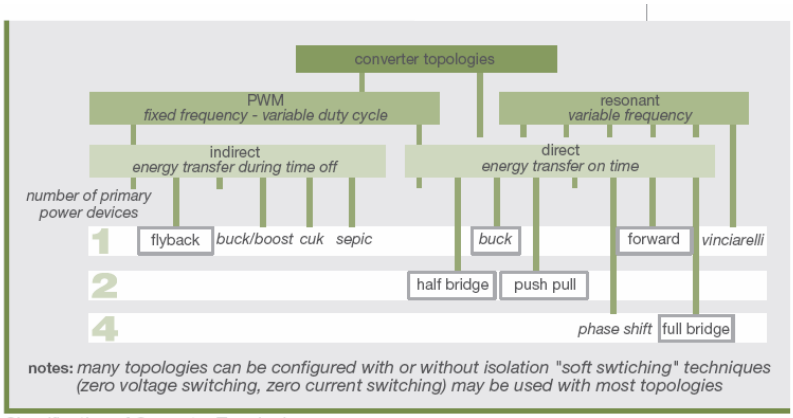
Fortunately, with the advent of standardized power modules, the end user does not need to analyze the topological choices in detail. The development of the standard DC/DC converter module as a component for implementation of decentralized power architectures allows the power system designer to focus on the final system characteristics of the module, such as reliability, efficiency, building height, and cost. The power system designer can then pay less attention to the internal details of the converter operation. We have, therefore, limited this section on topology to include only high level descriptions and comparisons.

A general classification scheme for topologies is presented, followed by a more detailed description of the topologies most commonly used in distributed converters. These commonly used topologies are then compared from a functionality and application point of view. Synchronous rectification, while not a topological distinction, is discussed as it pertains to the operational and cost characteristics of power converter modules. Finally, there is a discussion of multiphase converters that can enhance the performance of interconnected converter cells of various topologies.

2.4.3.2 Classification of Topologies

There is no universally accepted classification scheme for converter topologies. This is partly due to the large number of topologies that exist and also to the fact that similar topologies are referred to by more than one name. Rather than attempt to categorize and classify all possible topologies, we will only focus on the characteristics that are most meaningful to the end user and on the topologies that are actually used in commercially available DC/DC converter products.

The categorization of the most common topologies is shown in figure 2.4.3.1. The most fundamental distinction between topologies is the basic operating mode - either Pulse Width Modulated (PWM) or resonant.



Classification of Converter Topologies

Figure 2.4.3.1

In a PWM converter, the operating frequency remains fixed at a constant value, typically between 50 kHz and 1 MHz. The regulation function is accomplished by changing the duty cycle of the converter, the percentage of time that the converter's power switching devices are active. The fixed frequency has the benefit that any subsequent filtering, both inside the converter and at the load, will be done at a known frequency. The constant frequency is also convenient from an EMC point of view in that the fundamental frequency will not change and can more easily be predicted and designed for. In a PWM converter, there are dynamic switching losses when the power devices are turned on and also when they are turned off. These transition losses tend to limit the maximum operating frequency at which reasonable efficiency can occur. With good design and packaging techniques, PWM converters can be very efficient up to an operating frequency of about 2 MHz.

A resonant converter operates by changing its operating frequency, and regulates by means of the frequency dependent impedance characteristics of a series or parallel resonant LC circuit. This approach, in theory, removes the constraint of lower efficiency at higher operating frequencies. Because of this, there is continuing research being done on resonant approaches and new resonant topologies and implementations are being proposed in great numbers. For practical converters, the upper operating frequency remains below 5 MHz due to present limitations in components and packaging. The actual efficiency of commercially available resonant converters is in the same region as that of the better PWM designs utilizing conventional rectification. PWM designs utilizing synchronous rectification can exhibit even higher efficiencies. Consequently resonant designs as yet exhibit no practical efficiency advantage to the end user. In the future, as the component and packaging limitations are resolved, it is possible that high frequency resonant approaches will become increasingly popular and more commonly used due to the higher packaging density that may result. On the other hand, the use of the multiphase techniques that will be described later may raise the effective operating frequency of PWM converters and obviate this potential advantage for the resonant approach.

For PWM converters, power transfer to the converter secondary can occur either during the power device on time or during off time. In the first case, the converter is referred to as a direct converter. In the second case, it is called an indirect converter. There are several examples of each that are commonly used in available DC/DC modules, and these are indicated in figure 2.3.1. The topologies that we will discuss in more detail are outlined with a box. The topologies are listed in the figure according to the number of primary switching devices each normally uses. In general, a larger number of devices imply additional complexity and cost, but also a higher power handling capability.

DC/DC converters are available in both isolated and non-isolated versions. Isolation, as referred to here, is the absence of a DC circuit path from the converter input voltage source to the output return, and is accomplished by means of some form of transformer within the converter. Both isolated and non-isolated converters are useful devices, with isolated varieties being more popular due to their greater flexibility for system grounding and safety design. Many of the topologies shown here can be implemented as either isolated or non-isolated converters.

One benefit of the research into resonant topologies has been the development of 'soft switching' techniques. Using these approaches, some of the switching losses of PWM converters can be minimized by taking advantage of resonance effects at the switching time and turning the power devices on or off under controlled conditions. Zero Voltage Switching (ZVS) and Zero Current Switching (ZCS) are two commonly used terms that apply to these kinds of techniques. In return for additional complexity of design, slightly improved efficiencies are possible, especially at higher power levels. It should be noted that most converters using these techniques are PWM converters rather than resonant and as such operate at a constant frequency.

2.4.3.3 Description of Common Topologies

The most widely used topologies are the buck, the flyback, the forward, the push-pull, the half bridge and the full bridge. We will give an overview of each of these approaches. The information provided is very general and only the fundamental elements of the topology are shown. There is no attempt to include all of the features and details required for a practical implementation of the topology. For simplicity and consistency, the power switch is shown as a MOSFET transistor. While MOSFETs are presently the most commonly used device in the range of power levels under consideration, bipolar transistors or IGBTs could be substituted without loss of generality in describing the topologies.

The simplest converter topology is the buck. This topology can be implemented either as an isolated or non-isolated converter, but the non-isolated version as shown in figure 2.4.3.2 is by far the most popular and will be described here. The buck is a forward converter with energy transfer to the output occurring during the on time of switch Q1. Setting the output voltage as a function of the input voltage is done by changing the duty cycle (or duty ratio) of the converter. This is done with a feedback loop from the output that controls the converter duty cycle to maintain a fixed output voltage. As with the discussion of the other topologies, we will not include the feedback and control mechanisms in the simplified topology schematics shown here.

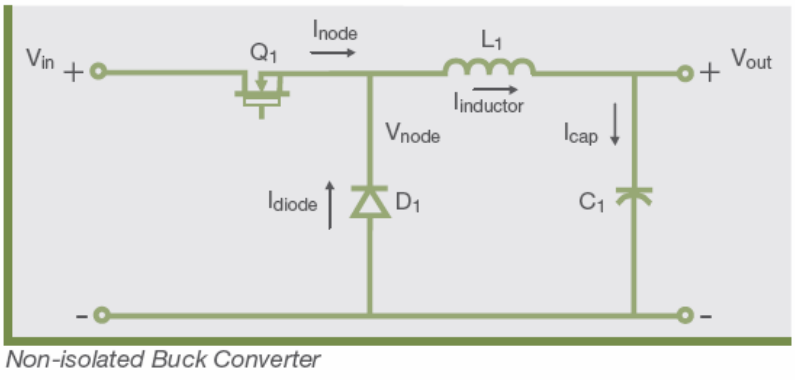


Figure 2.4.3.2

The fundamental operating voltage and current waveforms for the buck converter are shown in figure 2.4.3.3. During the Q1 on time, energy from the input voltage is transferred to the inductor L1, with diode D1 reversed biased and conducting no current. The inductor current supplies the output current as well as current to charge the output capacitor C1.

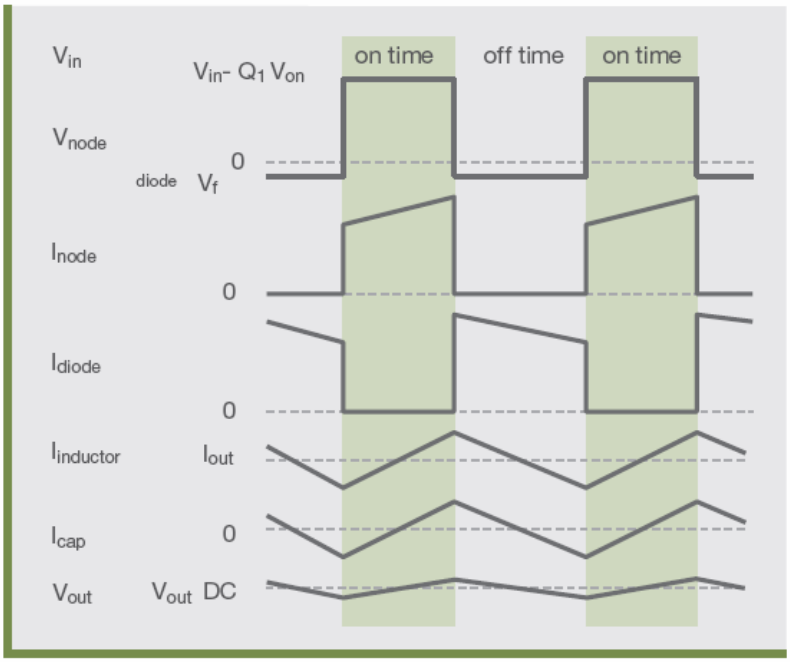


Figure 2.4.3.3

When Q1 switches off, the output section of the converter receives no additional energy from the input side. Load current continues to flow, however, supplied by the stored energy in L1 and C1. During the off time, the load current is re-circulated through L1 through the diode that is now forward biased. Consequently, the voltage at the Q1, L1, D1 node during the off time is set at one diode forward drop below the output ground. During the on time, this node voltage is equal to the input voltage less the on resistance voltage drop through Q1.

The inductor current has an average value equal to the converter output current, but supports a triangular AC component as the inductor current increases via Q1 during the on time and depletes through the load during the off time. The output capacitor current has an average value of zero, but has an appreciable AC ripple component that is equal to the inductor ripple current. The converter output ripple voltage also has a triangular waveform that it largely determined by the ESR of the output capacitor.

The buck topology is limited to down conversion, with the output voltage less than the input voltage source. The buck converter is primarily used in low power applications (less than 25 W) and is often used in battery powered applications to develop voltages less than the battery voltage. Many of the selfcontained switching regulator ICs utilize the buck topology.

The flyback converter is shown in figure 2.4.3.4. This is the only indirect converter that we will be discussing here. The uniqueness of this approach is that the transformer acts as an energy storage device during the converter operating cycle. During the switch on time, the output diode is reverse biased so that no current can flow into the secondary filter. During this time, the converter output current is provided by energy previously stored in the converter output capacitors and inductor. When the switch is turned off, the transformer polarity reverses, or ‘flies back’, and the energy stored in the transformer is released to the secondary.

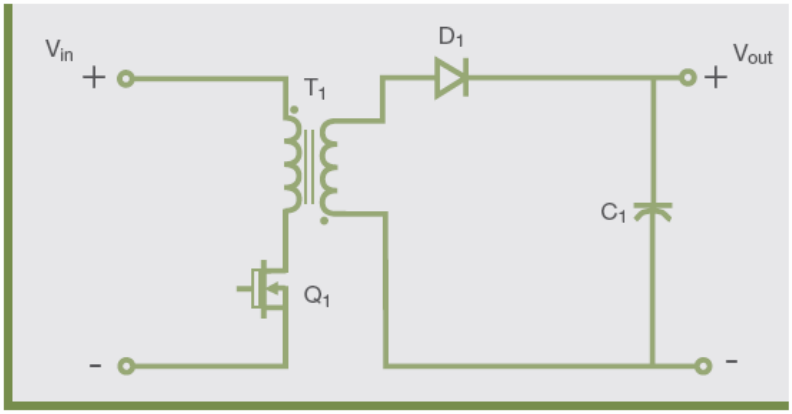


Figure 2.4.3.4

The flyback is a very simple topology in terms of number of components required. It is limited, however, in power handling capability due to the use of a single switching device and the voltage stress levels imposed on the switch. Most flyback converters are designed for applications of less than 100 W.

The forward converter, the simplest form of which is shown in figure 2.4.3.5, is a very common and versatile topology. It is a direct converter, so the energy from the input to output is transferred during the on time of the switch device. During this time, secondary diode D2 is reverse biased and current flows to the load through the secondary inductor. During the switch off time, the transformer primary voltage reverses polarity due to the change in primary current. This forces the transformer secondary to also reverse polarity. Secondary diode D2 now becomes forward biased, and conducts current through the load driven by the stored energy in the output filter inductor. The simple topology shown in the diagram is not practical for power levels above perhaps 100 W. However there are many extensions of the forward topology that permit cost-effective operation at higher power levels. Some of the more commonly used variations and extensions of the forward topology are the resonant reset forward and the two-transistor forward.

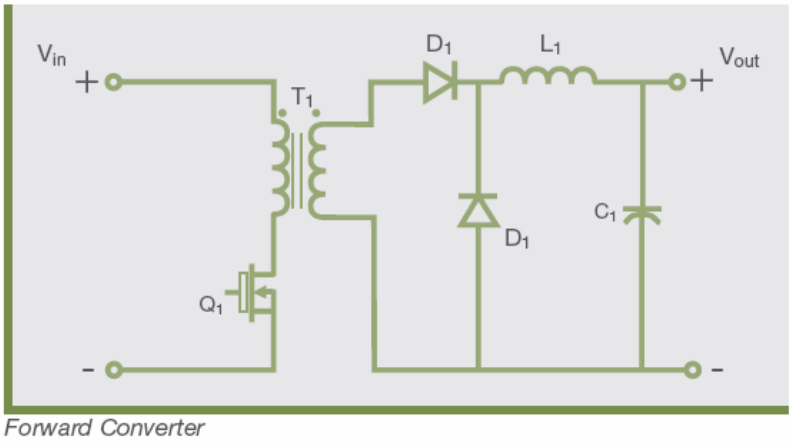
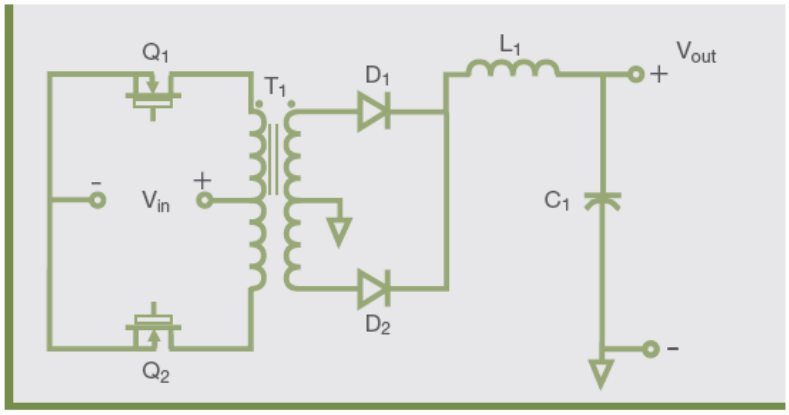


Figure 2.4.3.5

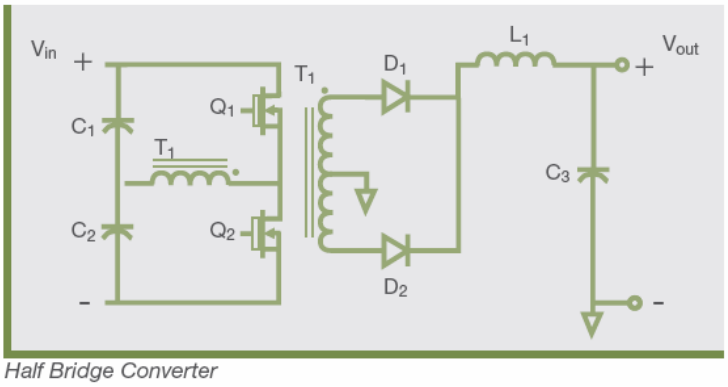
The push-pull converter is shown in figure 2.4.3.6. It is a two transistor topology that utilizes a tapped primary on the converter transformer. As each power switch conducts in turn during the operating cycle, the direction of current in the primary changes resulting in a bipolar secondary current waveform. The push-pull is most useful for lower input voltages, since each of the power switches is exposed to a voltage stress of two times the DC input voltage due to the tapped transformer primary.



Push-Pull Converter

Figure 2.4.3.6

The half bridge topology is shown in figure 2.4.3.7. This is a two switch direct converter. A voltage level of half the input voltage is generated by the two stacked capacitors on the input. The transformer primary is alternatively switched from this voltage to either V_{in} or input return, so that the transformer primary voltage is V_{in} / 2. In return for the additional complexity of the input capacitors, this topology exposes the power switches to a maximum voltage stress of V_{in} rather than 2Vin as with the push-pull. This allows the half bridge to be useful at higher power levels

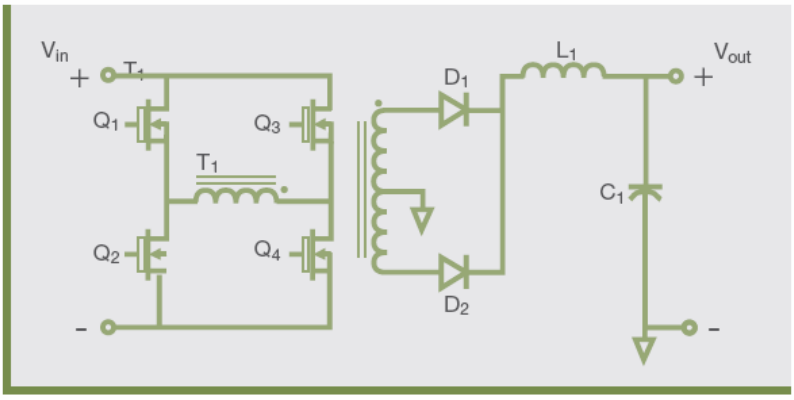


Half Bridge Converter

Figure 2.4.3.7

The full bridge converter is a direct converter using four switching devices, and is shown in figure 2.4.3.8. In this topology, diagonally opposite switches are simultaneously conducting, imposing the full input voltage across the primary winding of the transformer. During each half cycle of the converter, the pair of switches used changes, so that the polarity of the primary reverses. As in the half bridge, the maximum switch voltage stress is equal to Vin. At a given power level, the primary current and switch current is half that of the half bridge due to the higher primary voltage. This makes the full bridge suitable for higher

power levels. It is perhaps the most common topology for converters in the 400 to 2000 W power range..



Full Bridge Converter

Figure 2.4.3.8

As will be discussed in the chapter on converter selection, topology should not be a major criterion during selection of a standard DC/DC module. There is no one topology that is always best. For a given power level and other design considerations and constraints, there are one or more topologies that are suitable. The module supplier will select a topology based upon efficient design practices, availability of highly reliable components, good performance characteristics, and reasonable cost. Figure 2.4.3.9 provides a high-level comparison of the topologies we have presented.

Topology	Required number of power semiconductors	Device voltage stress (V)	Optimal power Level (W)	Comments
Flyback	2	V_{in} + N V_{out}	5 to 50	N = transformer turns ratio low complexity, low cost
Forward	3	2 V_{in}	15 to 150	many variations
Push-Pull	4	V_{in}	15 to 150	
Half bridge	4	V_{in}	15 to 200	
Full bridge	6	V_{in}	150 to 1500	

Comparison of Common Converter Topologies

Figure 2.4.3.9

2.4.3.4 Synchronous Rectification

One of the biggest recent improvements in efficiency of DC/DC converters has been due to the utilization of synchronous rectification in their design. Synchronous rectification does not constitute a new or different topology. It can be used with all of the topologies discussed above. We will discuss it in this chapter, however, because it is an important topic and can be a significant criterion for the selection of a standard BMPS.

Synchronous rectification is simply the substitution of a MOSFET device for a conventional silicon or Schottky rectifier. This substitution can enhance efficiency because the DC losses for the MOSFET will be lower over a fairly broad range of forward current. The forward DC losses for a conventional diode will be the forward current times the forward voltage drop (0.4 to 0.5 V for a Schottky device). The power dissipated by a conducting MOSFET will be equal to the device's on resistance times the square of the forward current. Modern low voltage MOSFET devices can have very low Rds-on ratings – 10 m? or less. Consequently, their forward conduction losses will be lower than that of even a Schottky diode for reasonable levels of current. These characteristics are shown in figure 2.4.3.10. Note that the

synchronous approach achieves a lower conduction loss until the crossover point with the linear losses of the diode. This crossover point will vary with the available MOSFET device technology at any given time, but is presently in the range of 80 A or so for single devices. Note that this analysis only addresses DC forward losses. The switching losses are equally real and significant for both diodes and synchronous rectifier MOSFETs. These losses are very design-dependent and will not be accounted for here.

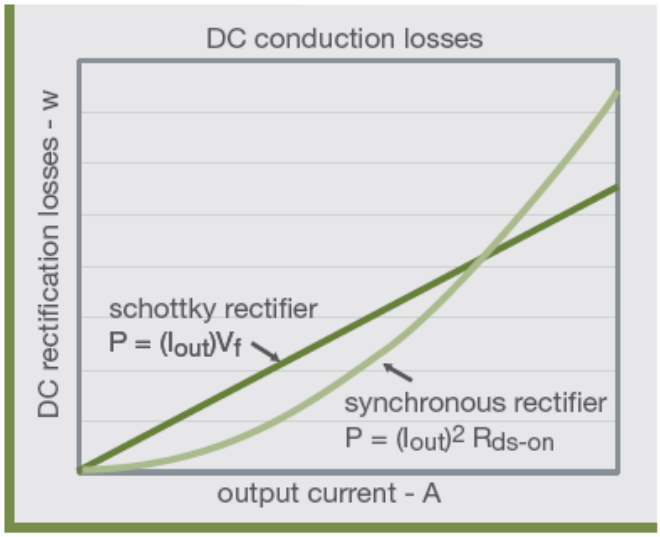
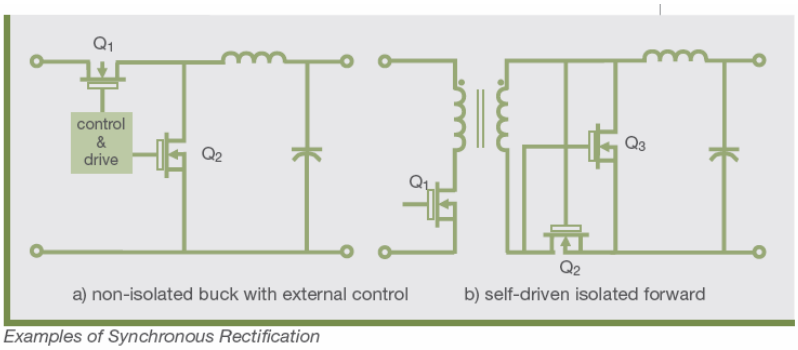


Figure 2.4.3.10

The synchronous rectification approach involves some increased complexity and cost as will be described shortly. Consequently, it is not often used at the very low end of the output current spectrum, say 10 A or less. The efficiency advantages of synchronous rectification are greatest at low output voltages. As a result, it is mostly used for converters with output voltages of 5 V or less with output currents between 10 and 80 A.

The additional complexity of synchronous rectification referred to above arises from the need to provide gate drive signals to the MOSFET(s) to control the conduction time. Unlike diodes, they are not self-commutating two terminal devices. The overall efficiency is determined by both the control of the on time of the MOSFET(s) relative to the operating cycle of the converter and the minimization of dynamic switching losses during turn on and turn off of the device(s). In general, achieving the highest levels of efficiency requires the use of more complex gate drive arrangements.

The two general categories of gate drive approaches are self-driven and external control. The self-driven approach is simpler and requires the use of less external components. The external control approach gives the converter designer greater flexibility in the turn on and turn off times and the generation of optimal gate-drive signals. An example of each approach is shown in figure 2.4.3.11. The synchronous non-isolated buck converter shown is an example of the usage of external control. The rectifier MOSFET, Q2, is driven by control and drive logic in a similar way to the main switching device Q1. This approach is easier to implement in non-isolated converters since the rectifier control and drive circuits do not need isolation from the primary-side control functions for the main switching MOSFET. The second example shows a basic isolated forward converter with a self-driven synchronous rectification design. In this design, the drive for the rectifier MOSFETs Q2 and Q3 is achieved by the polarity reversals on the transformer secondary. This achieves the ultimate simplicity of design, but with no control over the exact switching times or gate drive characteristics. Similar designs sometimes use an auxiliary winding on the transformer dedicated to the generation of the drive waveforms.



Examples of Synchronous Rectification

Figure 2.4.3.11

The DC/DC converter user should be aware of another characteristic of converters using synchronous rectification. In general, they cannot be directly paralleled without the use of isolation diodes. Thus, in architectures that require paralleling for increased current demand, the efficiency advantage of the synchronous rectification is at least partially offset by the losses inherent in the isolation diodes.

2.4.3.5 Multiphase Conversion

Multiphase converters are another recent trend that relates to topological issues. They are not a circuit topology, as they can be configured with arrays of converters of the topologies we have discussed above. They can be thought of as “Meta Topologies”, or arrangements of converter cells at the sub-system level to achieve advantages not possible with a single converter. A multiphase converter is an arrangement of two or more identical converters with their inputs and outputs connected in parallel and operating with fixed phase shifts relative to each other. The number of interconnected converters, n, is typically between 2 and 8. An example for n equal 3 is shown in figure 2.4.3.12. The operating cycle phase shift between converters is set to 360º / n, or 120º for the example shown. The three converters will share the total output power and current essentially equally, so that 33 W converters would be used for a 100 W load. Note that the effective output ripple frequency is multiplied by a factor of 3 and the ripple amplitude is reduced by the same factor. These are desirable and useful characteristics for the power system designer. The advantages of the multiphase approach include:

- Increased ripple frequency allows for smaller filtering components
- Less ripple amplitude
- Better dynamic response
- Smaller converter components allow for increased integration and lower packaging profiles
- Converter power dissipation is spread out over several components, allowing enhanced thermal performance on a PCB without heatsinks

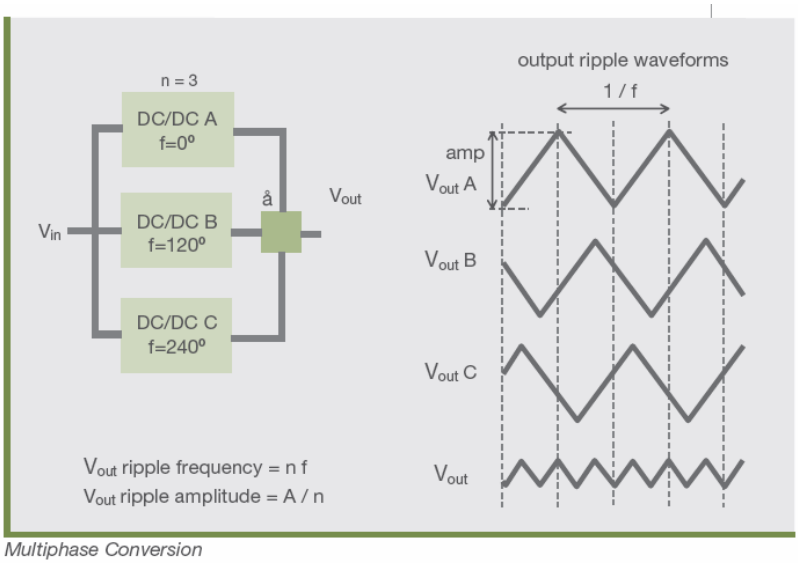


Figure 2.4.3.12

The potential disadvantage of this approach is the replication of converter cells, each composed of several components. Unless highly reliable components and manufacturing techniques are used, this could increase the failure rate for a given total converter output power. Fortunately, today's components and automated manufacturing are up to this challenge, and the multiphase approach will be seeing increasing usage in the near future. Presently, the largest use is in the latest non-isolated voltage regulator modules for high performance microprocessors. These devices use synchronous buck topologies in a multiphase arrangement with n equal 4.

2.4.4 Standard Versus Custom Power Supplies

Standard modular power conversion components are finally a practical and economical reality, a reality that opens up many exciting opportunities for today's power system designer. But before discussing the benefits of these standardized solutions, it is instructive to first examine the prior art – the traditional customized power system. As will be seen, the customized approach has many problems, financial and administrative as well as technical.

2.4.4.1 Introduction

Every piece of electronic equipment incorporates one or more power supplies. Many of these power supplies are typically custom designs that are developed to meet the unique voltage and current demands of the system. They are almost always solid-state switching regulators operating at a frequency of between 50 kHz and 1 MHz. Until recently, most all supplies for Information Technology and Industrial applications used the AC powerline as a source of power, but now more are using a battery supported DC bus structure such as the traditional Telecom architecture. For purposes of this discussion of custom power supply development and implementation, an AC powerline source will be assumed. We will follow the development and manufacturing start-up process for a typical custom power supply and observe some of the potential pitfalls along the way.

2.4.4.2 Product Definition

Before design can begin, requirements and specifications must be developed. The most important specifications are the voltage, current, and regulation requirements for the load circuits within the equipment. A partitioning of the load circuitry into cards, boards, equipment cabinets, etc. must also be